AMENDMENTS TO THE CLAIMS

1. (Original) A method for managing an error in a plurality of elements, the method comprising:

testing an element of the plurality of elements;

detecting the error in the element;

repairing a group of N elements of the plurality of elements, wherein N is greater than one and the group of N elements includes the element; and

inhibiting subsequent repairing of the group of N elements.

2. (Original) The method of claim 1 wherein the step of inhibiting comprises:

setting an inhibit flag which prevents the step of repairing from subsequently operating on elements of the group of N elements.

3. (Original) The method of claim 1 wherein the step of repairing comprises

invoking a group of replacement elements which is used in place of the group of N elements.

4. (Original) The method of claim 1 wherein:

the elements are memory elements of an array, and

the array comprises a plurality of rows and a plurality of columns.

5. (Original) The method of claim 4 further comprising:

initializing a row register and a column register to a first element in the array, prior to the step of testing.

6. (Original) The method of claim 4 wherein the step of inhibiting comprises:

checking, after detecting of the error, whether an inhibit flag which prevents the step of repairing from subsequently operating on elements of the group of N elements is set; and

if the inhibit flag has not been set, sending a row address of the element to row repair logic for performing the step of repairing and setting the inhibit flag; and

if the inhibit flag has been set, inhibit operation of the row repair logic.

7. (Previously Presented) The method of claim 6 wherein the rows are numbered from 0 to X(N-1) for a total of XN rows, and X is an positive integer, the method further comprising:

clearing the inhibit flag prior to the step of testing, if a row register is equal to a multiple of N.

8. (Original) The method of claim 4 wherein the step of testing comprises:

incrementing a column register and repeating the step of testing an array element until the last column of the row; and

incrementing a row register and repeating the steps of testing and incrementing the column register until the last row of the array.

9. (Previously Presented) A computer program product having a computer readable medium having computer program logic recorded thereon for managing an error in a plurality of elements, the computer program product comprising:

means for locating an error in one element of the plurality of elements;

means for replacing a group of N elements of the plurality of elements with replacement elements, wherein N is greater than one and the group of N elements includes the one element; and

means for inhibiting subsequent operation of the means for replacing the elements of the group of N elements.

10. (Original) The computer program product of claim 9, wherein the means for inhibiting comprises:

means for setting an inhibit flag which prevents the means for replacing from subsequently operating on elements of the group of N elements.

11. (Original) The computer program product of claim 9 wherein:

the elements are memory elements of an array, and

the array comprises a plurality of rows and a plurality of columns.

12. (Original) The computer program product of claim 11 wherein the means for inhibiting comprises:

means for checking, which is operative after location of an error, whether an inhibit flag which prevents the means for replacing from subsequently operating on elements of the group of N elements is set;

wherein if the inhibit flag has not been set, a row address of the element is provided to the means for replacing, and the means for inhibiting sets the inhibit flag; and

if the inhibit flag has been set, the means for inhibiting prevents operation of the means for replacing.

13. (Original) The computer program product of claim 11 further comprising:

means for testing an array element, which is operative, prior to the operation of the means for locating;

means for incrementing a column register and repeating the operation of the means for testing an array element until the last column of the row; and

means for incrementing a row register and repeating the operation of the means for testing and the means for incrementing the column register until the last row of the array.

14. (Previously Presented) The computer program product of claim 12 wherein the rows are numbered from 0 to X(N-1) for a total of XN rows, and X is an positive integer, the computer program product method comprising:

means for clearing the inhibit flag, prior to the step of testing, if a row register is equal to a multiple of N.

15. (Previously Presented) A system for preventing duplicate cache memory repairs in a memory array of a plurality of memory elements, the system comprising:

read circuitry that reads out the contents of a portion of the memory array, wherein the portion comprises at least two elements of the plurality of memory elements;

compare circuitry that compares the contents with expected contents and detects an error in the portion;

repair logic that repairs a group of N elements of the plurality of memory elements, wherein N is greater than one, and the group of N elements includes the portion; and

inhibit circuitry that prevents the repair logic from subsequently operating on the group of N elements.

16. (Original) The system of claim 15 wherein the inhibit circuitry sets an inhibit flag which is used to prevent the repair logic from subsequently operating on the group of N elements.

17. (Original) The system of claim 15 wherein the repair logic invokes a group of replacement memory elements which is used instead of the group of N elements.

18. (Original) The system of claim 15 wherein:

the array comprises a plurality of rows and a plurality of columns, and the portion is a row;

the inhibit circuitry determines, after detection of the error, whether an inhibit flag is set, which prevents the repair logic from subsequently operating on elements of the group of N elements; and

if the inhibit flag has not been set, a row address of the element is sent to the repair logic, and the inhibit circuitry sets the inhibit flag, and if the inhibit flag has been set, the inhibit circuitry prevents operation of the repair logic.

19. (Previously Presented) The system of claim 15 wherein:

the rows are numbered from 0 to X(N-1) for a total of XN rows, and X is an positive integer; and

the inhibit circuitry clears the inhibit flag prior to the operation of the compare circuitry, if a row register is equal to a multiple of N.